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EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,605	HARTZELL ET AL.	
	Examiner	Art Unit	
	David S. Kim	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. **Claims 1-7** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In particular, notice the following limitations in independent claims 1, 7, and 14:

(**claim 1**) "the metallic ground plane providing ***electrical isolation*** between the high-voltage power supply and the transmitter portion and the receiver portion"

(**claim 7**) "means for ***electrically isolating*** the means for generating the high-voltage bias from the means for receiving and the means for transmitting" (emphasis Examiner's).

However, the high-voltage power supply/means for generating the high-voltage bias provides a bias voltage, i.e., an ***electrical*** signal, to at least the receiver portion/means for receiving (Applicant's specification, paragraph [024]). The metallic ground plane/means for electrically isolating does not prevent this supply of an electrical signal from the high-voltage power supply/means for generating the high-voltage bias for at least the receiver portion/means for receiving. That is, the metallic ground plane/means for electrically isolating does not provide "electrical isolation"/"electrically isolating" between the high-voltage power supply/means for generating the high-voltage bias and at least the receiver portion/means for receiving. Furthermore, the disclosure does not provide any additional teachings to enable one of ordinary skill in the art to implement these limitations. Accordingly, these limitations of "electrical isolation"/"electrically isolating" constitute subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As a remedy, Examiner respectfully suggests Applicant to incorporate the terms "shield" and "shielding" and "electromagnetic signals emanating from the high-voltage power supply" instead of "electrical isolation"/"electrically isolating". That is, instead of providing "electrical isolation"/"electrically isolating", it appears more accurate to describe the metallic ground plane as shielding the transmitter portion and the receiver portion from electromagnetic signals emanating from the high-voltage power supply (paragraph [030]).

Specification

3. The disclosure is objected to because of the following informalities:

Similar to the enablement rejection under 35 U.S.C. 112, first paragraph, above, Applicant employs the terms "electrical isolation", "electrically isolating", and other similar terms where it may be more accurate to incorporate the terms "shield", "shielding", "electromagnetic signals emanating from the high-voltage power supply", and other similar terms.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 1, 3-9, and 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky et al. (U.S. Patent No. 4,766,471, hereinafter "Ovshinsky") in view of Ramaswami et al. (*Optical Networks: A Practical Perspective, 2nd ed.*, hereinafter "Ramaswami"), Stager et al. (U.S. Patent No. 5,777,383, hereinafter "Stager"), and Chou et al. (U.S. Patent Application Publication No. 2002/0140081 A1, hereinafter "Chou").

Regarding claim 1, Ovshinsky discloses:

A transceiver system, comprising:

a transmitter portion (e.g., 1st layer in Fig. 16A with transmitter elements of col. 30, l. 10-13) arranged on a bottom layer (1st layer in Fig. 16A would be on the "bottom" if viewed upside-down) of a multi-layer board (e.g., 540), the transmitter portion capable of providing signals to a transmitter optical subassembly;

a receiver portion (e.g., 1st layer in Fig. 16A with receiver elements of col. 30, l. 40-48) arranged on the bottom 1st layer in Fig. 16A with transmitter elements of col. 30, l. 10-13) layer of the multi-layer board (e.g., 540), the receiver portion capable of receiving signals from a receiver optical subassembly.

Ovshinsky does not expressly disclose:

a ***high-voltage power supply*** arranged on a ***top*** layer of the multi-layer board, the high-voltage power supply providing a ***bias voltage*** for the receiver optical sub assembly; and

a ***metallic ground plane*** arranged on a first intermediate layer between the top layer and the bottom layer, the metallic ground plane providing ***electrical isolation*** between the high-voltage power supply and the transmitter portion and the receiver portion.

Regarding the limitation of a ***power supply***, notice that one would obvious implement some kind of power supply for the various components of the apparatus of Ovshinsky.

Regarding the limitation of a ***high-voltage*** power supply, notice that Ovshinsky broadly discloses the use of various type of receiver elements (col. 30, l. 40-48). Another well-known type of receiver element is disclosed by Ramaswami, such as an avalanche photodiode (p. 197, APDs). At the time

the invention was made, it would have been obvious to one of ordinary skill in the art to employ other alternate types of receiver elements, such as an APD. One of ordinary skill in the art would have been motivated to do this for other benefits that they may have over other types of receiver elements. For example, an APD has greater responsitivity than other types of receiver elements (Ramaswami, p. 197, 1st full paragraph). An APD generally requires a ***high-voltage power supply for bias voltage***, so an obvious variation of Ovshinsky with an APD would also employ a ***high-voltage power supply for bias voltage***.

Regarding the limitations of arranging a power supply on a ***top*** layer of a multi-layer board, the ***ground plane***, and the ***electrical isolation***, notice that the practice of locating a power supply and other circuitry on opposite sides of a multi-layer board with a ground plane in between the power supply and this other circuitry is known in the art, as shown by Stager (Fig. 5, power planes 68, 70, and 72 and other circuitry on interconnect layers 52, 54, 56, and 58 with a ground shield layer in between the power planes and an interconnect layer, col. 5, l. 14-16). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to locate the power supply and the transmitter and receiver portions on opposite sides of the multi-layer board (power supply on the ***top*** layer) with a ground plane between the power supply and other circuitry, as exemplified by Stager. One of ordinary skill in the art would have been motivated to do this since doing so would result in the isolation of devices to prevent electromagnetic interference (Chou, abstract). Moreover, notice that ground planes are known to be metallic (Chou, paragraph [0053]).

Regarding claims 3-5, Ovshinsky in view of the references applied above (hereinafter the "RAA") does not expressly disclose:

(claim 3) The system according to claim 1, wherein a second intermediate layer having vias is arranged between the first intermediate layer and the top layer.

(claim 4) The system according to claim 1, wherein a third intermediate layer having vias is arranged between the first intermediate layer and the bottom layer.

(claim 5) The system according to claim 4, wherein an interconnect layer is arranged between the first intermediate layer and the third intermediate layer.

However, Ovshinsky does disclose the use of multiple layers (Ovshinsky, Fig. 16A), and the use of vias is well known for connecting multiple layers (Stager, vias in Fig. 5). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include any of these various layers and vias to provide obvious variants of the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this for any variety of suitable reasons, e.g., addition of components and circuitry.

Regarding claim 6, Ovshinsky in view of the RAA does not expressly disclose:

The system according to claim 1, further including a microcontroller system arranged on the top layer and the bottom layer.

However, the use of a microcontroller system for a system, such the system of Ovshinsky in view of the RAA, is an extremely well known practice in the art. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to place a microcontroller system on the top and bottom layers. One of ordinary skill in the art would have been motivated to do this to locate microcontroller components in close proximity of the circuits that they would control, such as the power supply of the top layer and the transmitter and receiver portions of the bottom layer.

Regarding claims 7-9, claims 7, 8, and 9 are claims that introduce limitations that correspond to the limitations all introduced by claim 1. Therefore, the recited limitations in claim 1 read on the corresponding limitations in claims 7-9.

Regarding claim 11, Ovshinsky in view of the RAA discloses:

The method of claim 8, further including arranging a first intermediate layer between the top layer and the bottom layer, the first intermediate layer including vias to provide electrical contact with traces on the top layer (e.g., Stager, vias in Fig. 5).

Regarding claims 12-13, Ovshinsky in view of the RAA does not expressly disclose:

(claim 12) The method of claim 11, further including arranging a second intermediate layer between the first intermediate layer and the intermediate layer, the second intermediate layer providing traces.

(claim 13) The method of claim 12, further including arranging a third intermediate layer between the intermediate layer and the bottom layer, the third intermediate layer including vias.

However, Ovshinsky does disclose the use of multiple layers (Ovshinsky, Fig. 16A). The use of vias is well known for connecting multiple layers (Stager, vias in Fig. 5). Also, the use of traces is also well known for connecting circuitry. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include any of these various layers, vias, and traces to provide obvious variants of the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this for any variety of suitable reasons, e.g., addition of components and circuitry.

Regarding claim 14, claim 14 is an apparatus claim that introduces limitations that correspond to the limitations introduced by system claim 1. Therefore, the recited means in apparatus claim 14 read on the corresponding means in system claim 1.

7. **Claims 2 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky in view of the RAA as applied to the claims above, and further in view of Nelson et al. (U.S. Patent No. 5,097,393, hereinafter "Nelson").

Regarding claim 2, Ovshinsky in view of the RAA does not expressly disclose:

The system according to claim 1, wherein the transmitter portion and the receiver portion are arranged in a split-ground arrangement.

However, electrical circuitry generally requires a connection to ground. Instead of connecting the transmitter portion and the receiver portion to a common ground, split-ground arrangements are known in the art, as shown by Nelson (col. 12, l. 26-52). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include such an arrangement in the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this to provide electrical isolation (Nelson, col. 12, l. 27-28), which generally reduces electrical interference between various components. For example, one could provide electrical isolation between the transmitter portion and the receiver portion to reduce electrical interference between these portions by employing a split-ground arrangement instead of a common ground arrangement.

Regarding claim 10, Ovshinsky in view of the RAA does not expressly disclose:

The method of claim 8, further including providing a split ground between the high-voltage power supply and the other circuitry.

However, electrical circuitry generally requires a connection to ground. Instead of connecting the high-voltage power supply and the other circuitry to a common ground, split-ground arrangements are known in the art, as shown by Nelson (col. 12, l. 26-52). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include such an arrangement in the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this to provide electrical isolation (Nelson, col. 12, l. 27-28), which generally reduces electrical interference between various components. For example, one could provide electrical isolation between the high-voltage power supply and the other circuitry to reduce electrical interference between these portions by employing a split-ground arrangement instead of a common ground arrangement.

Response to Arguments

8. Applicant's arguments, filed on 30 October 2007, with respect to Ovshinsky, have been fully considered but they are not persuasive.

Applicant states,

> "Claim 1 recites 'a transmitter portion arranged on a bottom layer of a multi-layer board, the transmitter portion capable of providing signals to a transmitter optical subassembly; a receiver portion arranged on the bottom layer of the multi-layer board.' Ovshinsky discloses 'two integrated circuit structures 540 and 542 [shown in Fig. 16A] each having multiple device planes, and each being equipped with one or more light-emitting DIFETs [Dielectrically-Isolated Field Effect Transistor] on the sides 544 and 546 of structures 540 and 542 respectively, said sides facing one another' (Column 30, lines 5-10). In Ovshinsky, optical information is transmitted from face 544 of structure 540 to face 546 of structure 542 (Column 30, lines 10-17). 'Thus, bidirectional optical communication between photo-active devices of the two structures is possible' (Column 10, lines 17-20). Thus, the transmitter face of Ovshinsky is a separate structure from the receiving face. This is in contrast to the limitation of claim 1 where the transmitter and receiver are arranged at the bottom layer of a multi-layer board. Therefore, the combination of Ovshinsky, Ramaswami, Peters, and Bartur fail to disclose, teach, or suggest both a transmitter and a receiver portion mounted on the bottom of the circuit board, as required by claim 1" (REMARKS, p. 5-6, bridging paragraph).

Examiner respectfully notes that face 546 and face 544 in Fig. 16A both have elements on the same plane/layer. Thus, a transmitter and a receiver are arranged on the same layer of a multi-layer board. Accordingly, this argument is not persuasive.

9. Applicant's arguments, filed on 30 October 2007, with respect to Peters (REMARKS, p. 6-7, bridging paragraph), have been considered but are moot in view of the new ground(s) of rejection. In particular, notice the application of new references to Stager and Chou.

10. Applicant's arguments, filed on 30 October 2007, with respect to Nelson, have been fully considered but they are not persuasive.

Applicant states,

> "Claims 2 and 10 are allowable over the combination of Ovshinsky, Ramaswami, Peters, Bartur, and Nelson for at least the reasons stated above. They are also allowable for the additional reasons stated below. The disclosure of Nelson is specific to power and ground plane arrangements disclosing that 'both the power plane (and the ground plane, if desired) can be split into several electrically isolated segments to deliver different power and reference voltages' (column 12, lines 26-29). This fails to disclose, teach, or suggest the system of claim 2 wherein the transmitter portion and the receiver portion are arranged in a split-ground arrangement. Nelson also fails to disclose, teach, or suggest the method of claim 10 wherein 'a split ground between the high-voltage power supply and the other circuitry' is provided" (REMARKS, p. 7-8, bridging paragraph).

In particular, notice the additional clarification of the application of Nelson provided in the treatment of claims 2 and 10 above. That is, electrical circuitry generally requires a connection to ground. Instead of connecting various electrical components and circuitry to a common ground, split-ground arrangements are known in the art, as shown by Nelson (col. 12, l. 26-52). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include such an arrangement in the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this to provide electrical isolation (Nelson, col. 12, l. 27-28), which generally reduces electrical interference between various components. For example, one could provide electrical isolation between the various electrical components and circuitry to reduce electrical interference between these portions by employing a split-ground arrangement instead of a common ground arrangement. Accordingly, this argument is not persuasive.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kobayashi et al. (U.S. Patent Application Publication No. 2003/0127704 A1) is cited to show a grounded shield layer that electrically separates components from each other to prevent both sides from influencing each other (shield layer in Figs. 11 and 12, paragraphs [0116], [0119], and [0121]).

Tanabe et al. (U.S. Patent No. 7,049,676 B2) is cited show a shielding layer in a telecommunication device (e.g., 150 in Figs. 7 and 8, col. 5, l. 17-40).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER